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GaAs MESFET Logic with 4-GHz Clock Rate

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Abstract—**Monolithic digital IC's with GaAs MESFET's have been built and operated at clock frequencies up to 4.5 GHz. The fabrication process uses selenium-implanted n-channels and a two-level Cr-Pt-Au metallization with 1-μm linewidth and 1-μm alignment tolerances. NOR gates with 86-ps propagation delay and 40-mW power consumption have been realized. Binary frequency dividers have been designed with master-slave flip-flops operating from dc up to an average maximum frequency of 4 GHz. In addition, more complex circuits have been integrated on single chips. A general-purpose octal counter with input gating and output buffering and an 8-bit multiplexer/serial data generator exhibit stable and reliable operation.**

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I. INTRODUCTION

IN OUR increasingly digital world, there is a strong trend toward higher and higher data processing speed. For example, future test and measurement systems will require:

1) direct measurement of signal frequencies from dc to several gigahertz via digital frequency division;

2) measurement of single-event time intervals with subnanosecond resolution;

3) synthesis of microwave frequencies with phase-locked loops incorporating digital frequency dividers;

4) generation and detection of pulses with less than 100-ps transition time at data rates of several gigabits per second.

To meet these objectives, medium-scale integrated circuits with logic gates having less than 100-ps propagation delay must be realized. This performance can be achieved with either GaAs transferred-electron devices (TED's) [1], [2] or GaAs metal-semiconductor field-effect transistors (MESFET's) [3]-[8]. In choosing between these two technologies, special consideration was given to repeatability and control of active device parameters in processing, high noise immunity, minimum jitter in pulse-waveform generation, availability of buffer amplifiers on the chip, stable operation independent of clock pulse width, and reliable performance without individual adjustment of bias voltages or circuit parameters for each chip. Considering these criteria, the technology with normally on (depletion-mode) GaAs MESFET's was selected as a general approach to highest speed logic.

The primary objective of this work was to design and build digital circuits that demonstrate stable, oscillation-free operation from dc up to a bit rate that is at least twice the rate of present highest speed silicon circuits. The secondary objective was to minimize power per logic gate without sacrificing speed. The intent was to integrate circuits of sufficient complexity on a single chip to perform practical, useful electronic functions. To reach this goal, the IC fabrication yield and processing control of MESFET parameters had to be significantly improved. A specific improvement over previously reported results [4] is a twofold increase in the clocking rate of binary frequency dividers. This was accomplished with a circuit layout that reduced parasitic capacitances and with a higher speed master-slave flip-flop design. For this design, the time required to alter the flip-flop's states is only one propagation delay.

The purpose of this paper is to review and discuss these recent advances in GaAs MESFET logic technology. Section II deals with material preparation and integrated circuit fabrication. Sections III-V are devoted to the design, layout, testing, and performance of basic logic gates, master-slave flip-flops, and more complex circuits such as a counter/timer and an 8-bit multiplexer. Section VI presents conclusions and an outlook to future improvements.

II. IC Fabrication

Practical IC fabrication requires that MESFET parameters be very uniform over the wafer area and reproduced with good control from wafer to wafer. Critical parameters are the pinchoff voltage[1] V_p, the saturated drain current I_{DSS}, and the drain-source on-resistance R_{dso}. A successful approach to achieve this objective has been the use of Se implantation into high-purity buffer layers [9]. The buffer layers are grown 2 μm thick on the ⟨100⟩ face of Cr-doped substrates using liquid phase epitaxy. Typical Hall mobilities are 8000 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at room temperature and greater than 100 000 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at 77 K. Se ions are implanted at 350°C substrate temperature with 500-keV energy up to a total dose of 4.5×10^{12} cm^{-2}. The samples are annealed at 850°C under a Si_3N_4 protective coating. The resulting n-type layers typically show 70-percent doping efficiency, 2×10^{17}-cm^{-3} peak electron concentration, 4500-$cm^2 \cdot V^{-1} \cdot s^{-1}$ Hall mobility, and 500-Ω/□ sheet resistance, with ±3 percent uniformity over a 1-in^2 wafer area. The essential features for the control of V_p, I_{DSS}, and R_{dso} are the high uniformity in sheet resistance, the well-controlled doping profile, and a reproducibly high mobility at the n-to-buffer-layer interface.

The circuit processing starts with the formation of Au-Ge ohmic contacts alloyed at 460°C. The resulting contact resistance ranges between 2×10^{-6} and 1×10^{-5} $\Omega \cdot cm^2$. A mesa etch, 0.3 μm deep, removes the conductive layer between the devices and provides electrical isolation. The gate is a Cr-Pt-Au stripe, 1 μm long, 0.4 μm thick, and typically 20 μm wide, that is delineated by a photoresist lift-off process. A SiO_2 layer is deposited on the wafer and via openings with tapered edges are chemically etched. The second metallization layer, consisting of Cr, Pt, and Au, is E-beam evaporated. The surface is then masked with resist and etched by argon ion-beam milling. The remaining metal forms an accurately delineated pattern of anodes for Schottky diodes, interconnection lines, and contact pads. Fig. 1 shows schematically a cross section of an IC with a MESFET, Schottky diode, and interconnection with crossover. In applying this process with five contact masking steps, a fabrication yield in excess of 20 percent was obtained for the MSI circuits described in Section V.

Typical electrical characteristics for a MESFET with 1-μm gate length and 20-μm gate width are listed in the following table.

Parameter	Symbol	Value	Bias Conditions V_{GS} (V)	Bias Conditions V_{DS} (V)
Pinchoff voltage	V_p	2.5 V	0	0
Saturated drain current	I_{DSS}	4 mA	0	2
Drain-source on-resistance	R_{dso}	240 Ω	0	0
Transconductance	g_m	2 mmho	0	2
Gate-source capacitance	C_{gs}	0.02 pF	0	2
Current-gain bandwidth	f_T	15-18 GHz	0	2
Open-circuit voltage gain	μ	10	0	2

III. High-Speed MESFET Logic Gates

High-speed, general-purpose GaAs MESFET logic gates capable of implementing two levels of logic (NAND and NOR) in about 100 ps with a fan-out of 2 have been built and characterized. These logic gates, which form the basis of the GaAs MESFET MSI logic family, were tested and characterized with five-circuit ring oscillator chips. Variation of speed with pinchoff voltage, device width, and temperature for NAND and NOR circuits was studied.

MESFET logic gates can be designed in a variety of two-, three-, and four-input configurations. The use of both series

[1] The term "pinchoff voltage" is here synonymous with gate-source cutoff voltage, the gate voltage at which $I_{DS} = 0.01\, I_{DSS}$.

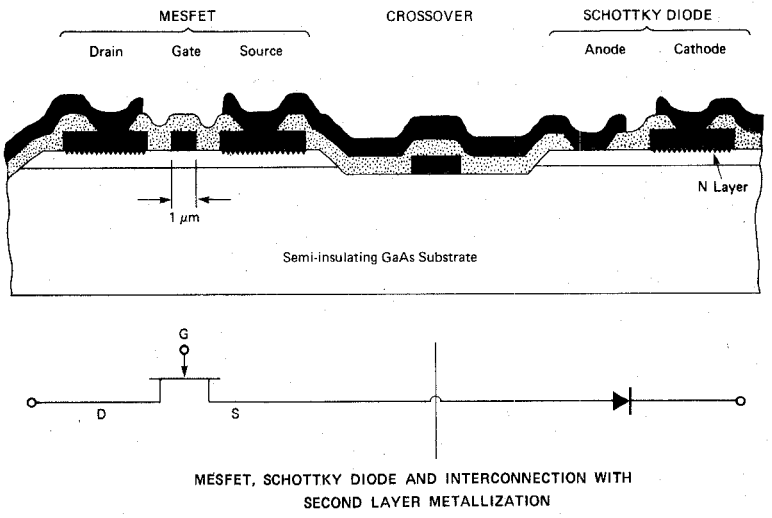

Fig. 1. Cross section of IC showing a MESFET, Schottky diode, and crossover connection.

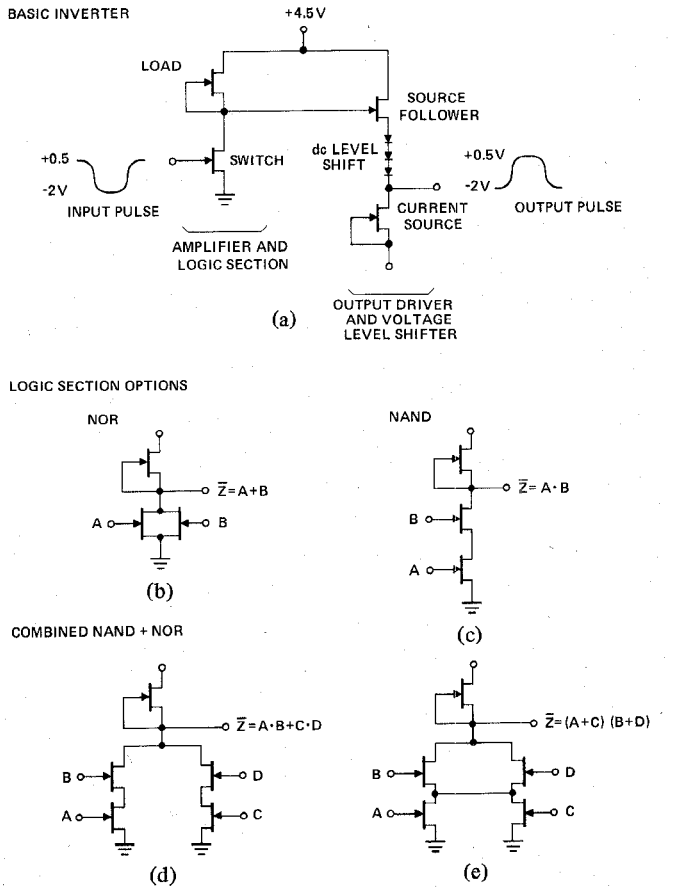

Fig. 2. High-speed MESFET logic gate. Inverter with output driver/level shifter (a), logic section options for NAND, NOR, and NAND + NOR functions (b)–(e).

and parallel connection of devices within the logic cell facilitates the design of both NAND and NOR functions, as well as EXCLUSIVE OR and INCLUSIVE AND circuits. A complete logic circuit is shown in Fig. 2. The current-sourcing load in this circuit is a high-impedance active load which consists of a MESFET with gate connected to source. The gate width of this load is chosen to be less than that of the switch MESFET in order to place the high-gain transition region near the center of the logic swing. Since the load is fabricated in the same way as the switch, the circuit is somewhat invariant to device

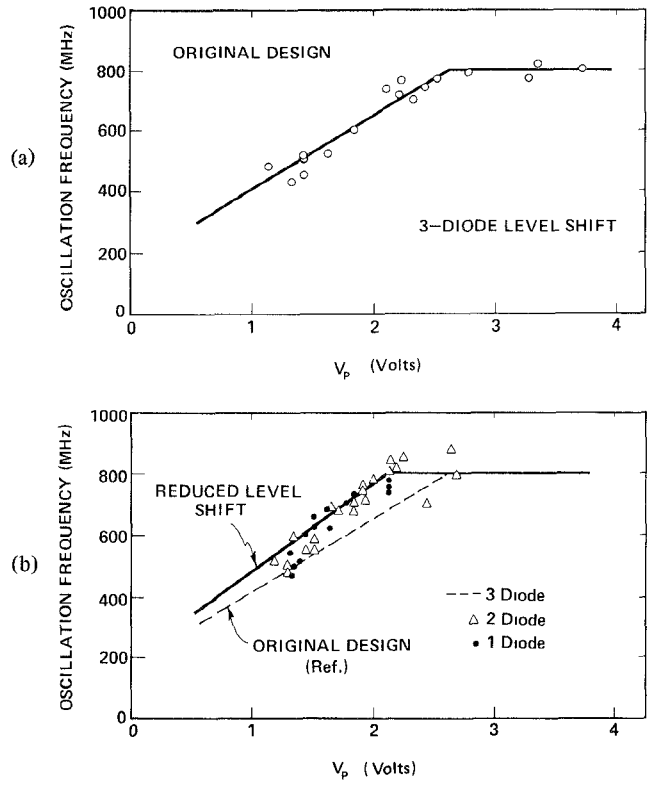

Fig. 3. Dependence of ring oscillator frequency on pinchoff voltage for original three-diode level shift circuit is shown in (a). Effect of reducing the number of level shift diodes is shown in (b).

parameter changes. With the active load, the circuit has a dc gain of 6 in its linear region and dc noise margins of about 1 V. The high-impedance node where load and switch connect is, however, highly susceptible to capacitive loading. For this reason, a buffer circuit must be incorporated into the logic gate to provide a low output impedance which is relatively insensitive to capacitive loading if the maximum circuit speed is to be obtained.

Since the MESFET, unlike the enhancement mode MOSFET, is a depletion mode device, a level shift is required to make the input and output voltage levels of the logic circuit compatible. This level shift is easily provided with the incorporation of Schottky diodes into the output buffer circuit. The number of diodes required is determined by the pinchoff voltage of the switch MESFET, and in turn determines the magnitude of the logic swing. Typically, three level-shift diodes are used in conjunction with -2.5-V pinchoff MESFET's to produce a gate with +0.5-V to -2.0-V logic swing. Fewer level-shift diodes can be used in conjunction with lower pinchoff MESFET's to make a circuit with somewhat less power consumption, smaller logic swing, and noise margins. It should be noted that although the three-diode level shifter consumes about 80 percent of the power in this design, up to three levels of logic (e.g., sum of three products) can be performed per level shifter, with consequent reduction of power per logic function.

The ring oscillator characterization of MESFET logic gates has revealed two important facts.

1) Propagation delay depends strongly on the pinchoff voltage of the switching MESFET's. Pinchoff voltage is itself a strong function of conductive layer thickness.

2) As circuit size (i.e., MESFET width) is reduced with layout rules unchanged, propagation delay increases. Circuits with very narrow gate width (and correspondingly low power consumption) approach the situation where propagation delay is inversely proportional to power, and a constant minimum power-delay product exists. Circuits with wide MESFET's approach a constant, minimum propagation delay.

The first effect, a strong dependence of circuit speed on pinchoff voltage, is illustrated in Fig. 3. This is a plot of oscillation frequency versus pinchoff voltage for one type of ring oscillator on a wafer where large pinchoff voltage variation exists, due to n-layer nonuniformity. Notice that below a pinchoff voltage of about 2.6 V, oscillation frequency is proportional to pinchoff voltage. As pinchoff voltage increases, so does the current available to charge and discharge the capacitance at the sensitive drain node. Since the rate of voltage change at this node is proportional to this current, F_{osc} increases with increasing V_p. The logic swing, however, is limited by the nonlinearity of the circuit, the magnitude of the swing being related mainly to the positive supply voltage, and independent of V_p. When the pinchoff voltage exceeds the magnitude of the logic swing (about 2.5 V), the switch transistors will not be completely cut off, so that the available current *change* at the drain node becomes limited by the amplitude of the logic swing, and is no longer proportional to V_p. When this happens, speed reaches a maximum, and further increase of V_p is only wasteful of power. Experiments

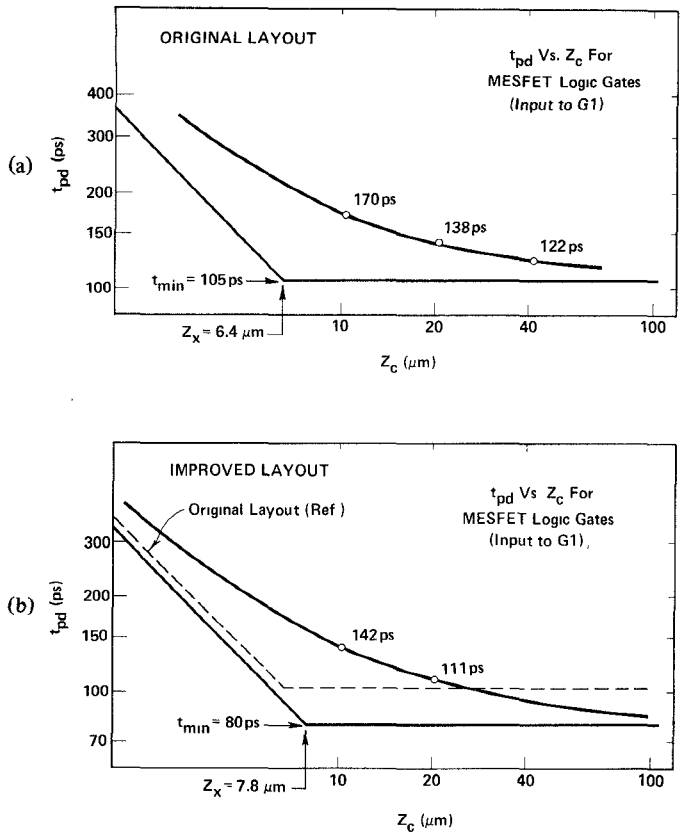

Fig. 4. Propagation delay t_{pd} versus gate width Z_c of MESFET's in NAND + NOR logic gate. Speed is limited by parasitic capacitance, and severely degraded at small Z_c by fringing component of this capacitance (a). Improved layout reduces capacitance and improves speed (b).

have shown that this threshold for maximum speed can be lowered about 0.5 V, from 2.6 V to 2.1 V, if either one or two diodes are used in the level shifter, with a corresponding decrease in supply voltage and a more limited logic swing [Fig. 3(b)]. Adoption of a two-diode design would allow operation at a lower supply voltage and allow acceptance of lower pinchoff units with maximum speed. These two power reducing features would be obtained at the expense of smaller logic swing and reduced noise margins.

The second point with regard to MESFET logic gate speed is the increase in propagation delay which is encountered as MESFET width is decreased. The motivation to decrease device width is mainly the desire for lower circuit power. MSI packing densities require per-gate power consumption of less than 50 mW, so that a useful amount of circuitry can be realized on a chip with total power dissipation of 1 W or less. Fig. 4(a) shows the relationship between propagation delay and MESFET gate width Z_c. The data, obtained from an early circuit layout, are for gate widths of 40, 20, and 10 μm. They are fitted to the curve

$$t_{pd} = t_{\min}\left(1 + \frac{Z_x}{Z_c}\right) \tag{1}$$

where

$t_{\min}$ = asymptotic minimum propagation delay

Z_c = MESFET gate width

Z_x = an experimentally determined constant.

This formula illustrates the fact that propagation delay (t_{pd}) approaches a minimum value ($t_{\min}$) for large gate widths ($Z_c >> Z_x$). For small gate widths ($Z_c << Z_x$), t_{pd} approaches the Z_x/Z_c asymptote, and propagation delay increases in inverse proportion to Z_c.

Note that the Z_x/Z_c asymptote is also the minimum power-delay product asymptote, since power is proportional to Z_c for a given pinchoff voltage. The speed-power tradeoff is clear: maximum speed demands wasteful expenditures of power, and minimum power-delay product requires the smallest possible layout.

To understand the reason for this effect, consider the simple case of a MESFET on a semi-insulating substrate. The current which flows between source and drain is clearly proportional to Z_c, since it is confined completely to a channel Z_c wide. The electric field, both laterally between source and drain and vertically to the grounded back plane, has fringing components which are independent of Z_c. This means that the drain-to-grounded-source capacitance, in addition to its proportionality to Z_c, includes a fixed fringing capacitance due to the fringing components of electric field emanating from the drain. The current available to charge this capacitance, however, is proportional to Z_c.

If the drain-to-source capacitance is

$$C_{DS} = \alpha(Z_c + Z_x) \tag{2}$$

and the switched drain current is

$$\Delta I_{DS} = \beta(Z_c), \tag{3}$$

then the time required to charge C_{DS} to a voltage ΔV with a constant current ΔI_{DS} is

$$t_{pd} = \frac{C_{DS} \cdot \Delta V}{\Delta I_{DS}} = \frac{\alpha}{\beta}\frac{Z_c + Z_x}{Z_c}\Delta V \tag{4}$$

or

$$t_{pd} = t_{\min}\left(1 + \frac{Z_x}{Z_c}\right) \tag{5}$$

where

$$t_{\min} = \frac{\alpha}{\beta} \cdot \Delta V. \tag{6}$$

It can be seen that it is necessary to minimize fringing capacitance to improve the minimum power-delay asymptote, and to minimize the per-unit gate width capacitance and maximize the switching current for a given voltage swing to achieve the lowest propagation delay limit.

Fig. 4(b) shows the improvements in both minimum delay asymptote and minimum power-delay product asymptote which are achieved by decreasing the area of source contact, drain contact, and interconnection metal within the logic gate to the smallest size compatible with the existing process design rules. Further layout reduction and consequent speed increase will be possible with improved process methods.

The sensitivity of logic gate propagation delay to temperature change was measured by monitoring ring oscillator frequency. The temperature coefficients are

measured oscillation frequency: -1.84 MHz/C°
corresponding propagation delay: $+0.22$ ps/C°
} 0.2 percent/C°.

This change in propagation delay is accompanied by a similar percentage change in power supply currents. It is known from measurements on discrete MESFET's that saturation current decreases with increased temperature, but pinchoff voltage remains constant. The resulting decrease in transconductance must be largely responsible for the temperature-induced speed degradation of logic circuits.

A summary of performance data for GaAs MESFET logic gates is given in the following table.

Property/Conditions	Circuit Type	Gate Width Z_c 20 μm	10 μm
Propagation Delay (fan-out = 2)			
Fig. 2(d):	NAND/NOR Gate Lower MESFET Input	111 ps	142 ps
	Upper MESFET Input	98 ps	–
Fig. 2(b):	NOR gate	86 ps	–
Power Consumption	Both Types	40 mW	20 mW
Average Power–Delay Product	Both Types	3.9 pJ	
Temperature Coefficient of Delay	NAND/NOR Gate G_1 Input	0.2 percent/C°	
Layout Area	Both Types	7000 μm^2	7000 μm^2 (not minimized)

IV. Frequency Dividers

Many high-frequency logic applications are based on binary counting (or frequency dividing) circuits.

The method chosen for implementing frequency division with GaAs MESFET logic was the master-slave flip-flop, a well-known circuit type which became popular with the advent of monolithic IC's. Advantages of the master-slave flip-flop approach are as follows.

1) Precise divide-by-two action. The exact number of input pulses is registered, and the division ratio is always exactly known.

2) Ability to handle any input frequency from dc to maximum counting frequency.

3) Ability to count frequency-modulated or pulse-modulated RF signals.

4) Triggerable by a waveform of any duty factor—does not require narrow pulse drive.

The first three advantages are not shared by narrow-band frequency dividers such as tunnel diode, Gunn diode, or harmonic phase-locked loop types. The fourth is an advantage over simple counting flip-flops with dynamic energy storage, such as the Eccles-Jordan bistable multivibrator with inductive or capacitive information storage, or self-oscillating delay-line type set-reset flip-flops.

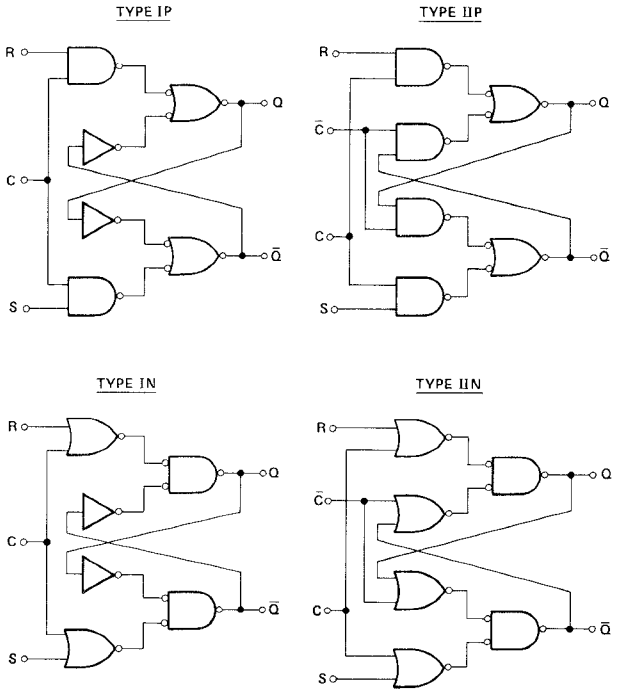

Fig. 5. Examples of the four basic cells which can be used in master-slave flip-flop design. Type I requires $2t_{pd}$ from application of clock until output is stable; Type II requires only $1t_{pd}$. (t_{pd} is propagation delay of NAND/NOR gate, from R to Q, for example.) Type P responds to positive clock level, Type N to negative clock level.

A master-slave flip-flop consists of two flip-flop cells, the outputs of the master feed the data inputs of the slave, and the inverted slave outputs feed the data inputs of the master when divide-by-two operation is desired. Any of the four basic data storage cells shown in Fig. 5 can be used as either master or slave in a master-slave flip-flop. The Type I cell stores data in a set-reset flip-flop (or latch), formed by the positive feedback connection of the NAND/NOR gates, which is active at all times. In the Type II cell, the data storage latch is active only during the portion of the cycle when the data storage command ($\bar{C}$ in Fig. 5) is activated. During the data entry phase (C activated), the storage latch is disabled. Because the storage latch is disabled, data entry in a Type II cell requires only one NAND/NOR propagation delay (e.g., from R to Q in Fig. 5). The Type I cell requires two gate propagation delays to reach equilibrium after activation of the data entry command, due to the additional time required for the signal to propagate through the feedback loop to override the state of the storage latch.

Although the Type II cell is twice as fast as the Type I cell, it is subject to data loss when both the data entry and data storage commands are deactivated. For example, in a IIP cell, if both C and $\bar{C}$ are below the activation threshold (approximately the center of the logic swing), then none of the four NAND gates in the IIP cell is capable of forcing either output low. Thus, the only possible states for Q and $\bar{Q}$ are high, and the state of the latch when the data storage com-

mand goes high is indeterminate. Caution must therefore be used in applying the Type II cell. The C and $\overline{C}$ inputs must not be allowed to simultaneously be below their activation thresholds for times much in excess of a propagation delay, or data loss will result.

Type I and Type II cells can be constructed in such a way that data entry and data storage phases are activated by a positive clock voltage (Type P) or by a negative clock voltage (Type N). Type IIN, for instance, refers to a cell with inhibited latch type data storage which activates upon application of a negative level at input C.

Master-slave flip-flops can be constructed by combining any of the four basic flip-flop cell types. Designation of a master-slave flip-flop as, for example, Type IIP-IIN, means that the master cell is Type IIP and the slave cell is Type IIN. There are two problems which can afflict master-slave flip-flops of this type. The previously discussed problem of data loss, which is peculiar to those circuits made with Type II cells, is avoidable by proper control of clock voltage bias. The second problem, self-oscillation, is common to circuits where both master and slave are of the same type, P or N (e.g., IP-IP) and the flip-flop is connected to form a binary frequency divider. Self-oscillation is not peculiar to high-frequency master-slave dividers or to the GaAs MESFET technology, but is solely due to the logical instability of a master-slave frequency divider when C and $\overline{C}$ are simultaneously active.

To understand self-oscillation, refer to the following table of logical equations and states for a master-slave frequency divider with active C and $\overline{C}$.

Logical Equations:

$$Q_{\text{MASTER}} = \overline{(Q_{\text{SLAVE}})} \cdot \overline{(\overline{Q}_{\text{MASTER}})}$$

$$\overline{Q}_{\text{MASTER}} = \overline{(Q_{\text{MASTER}})} \cdot \overline{(\overline{Q}_{\text{SLAVE}})}$$

$$Q_{\text{SLAVE}} = \overline{(\overline{Q}_{\text{SLAVE}})} \cdot \overline{(\overline{Q}_{\text{MASTER}})}$$

$$\overline{Q}_{\text{SLAVE}} = \overline{(Q_{\text{MASTER}})} \cdot \overline{(Q_{\text{SLAVE}})}$$

Table of States:

Node		State							
	0	1	2	3	4	5	6	7	0
Q_{SLAVE}	0	0	0	0	1	1	1	0	0
$\overline{Q}_{\text{SLAVE}}$	1	1	1	0	0	0	0	0	1
Q_{MASTER}	0	0	1	1	1	0	0	0	0
$\overline{Q}_{\text{MASTER}}$	1	0	0	0	0	0	1	1	1
		← Oscillation Period → = 8 Propagation Delays							

Assuming a typical set of initial conditions, it can be seen that the circuit spontaneously progresses through eight different states before repeating itself. The time between states is one gate propagation delay, t_{pd}. The waveform observed at any point has a $\frac{5}{8}$ or $\frac{3}{8}$ duty factor, with a period of $8 \times t_{pd}$. The self-oscillation mode will be defeated if either C or $\overline{C}$ is deactivated (held low in the case of Type P circuits). In mixed type circuits, such as IP-IN, the master clock is automatically deactivated when the slave clock is activated and vice versa, so the frequency divider is theoretically incapable of self-oscillation. In practice, however, there is a small range of clock voltages near the center of the logic swing where self-oscillation may occur with mixed type dividers, due to the imperfectly abrupt transfer characteristic of the logic gates.

Master-slave frequency dividers of Types IP-IP, IP-IN, IIP-IIP, and IIP-IIN have been monolithically integrated with the GaAs MESFET MSI technology. Fig. 6 shows an example of a divider chip containing the Type IIP-IIP divider along with attenuating output buffer circuits. All chips are 400 μm × 440 μm with a standard eight-pad configuration suitable for wafer probing with a special high-frequency microstrip probe card. The gate width of MESFET's in the four constituent NAND/NOR gates is 20 μm. Total power consumption is 160 mW for the divider circuit. First metal layer interconnect lines are 2 μm wide, second metal lines are 4-8 μm. General properties observed for the various divider types are summarized in the following table.

Frequency Divider Type	Advantages	Disadvantages
IP-IP	1) Completely immune to data loss.	1) Will self-oscillate. 2) Requires two-phase clock. 3) Typical maximum counting frequency = 2 GHz.
IP-IN	1) Generally will not self-oscillate. 2) Requires only one-phase clock. 3) Completely immune to data loss.	1) Typical maximum counting frequency = 2 GHz.
IIP-IIP	1) Typical maximum counting frequency = 4 GHz.	1) Will self-oscillate. 2) Requires two-phase clock.
IIP-IIN	1) Self-oscillates only over a narrow range of clock biases. 2) Typical maximum counting frequency = 3 GHz.	1) Requires two-phase clock.

It can be concluded from these observations that for ease of operation (one-phase clock, no self-oscillation, complete immunity to data loss) at restricted frequencies, IP-IN is the best choice. For maximum counting frequency (4 GHz typical), a particular circuit of the logical type IIP-IIP was most successful.

Although the Type IIP-IIP (and IP-IP) dividers could be forced to self-oscillate when both C and $\overline{C}$ were high, the problem was eliminated for realistic clock biases by offsetting the switching thresholds of data entry gates and latches in such a way that master and slave are not simultaneously susceptible to self-oscillation. This threshold offset, which was accomplished by altering the width of appropriate MESFET's within the circuit, allowed the IIP-IIP divider to operate properly at low frequency with slow-rising clock inputs, as well as at high frequency (Fig. 7). In particular, this IIP-

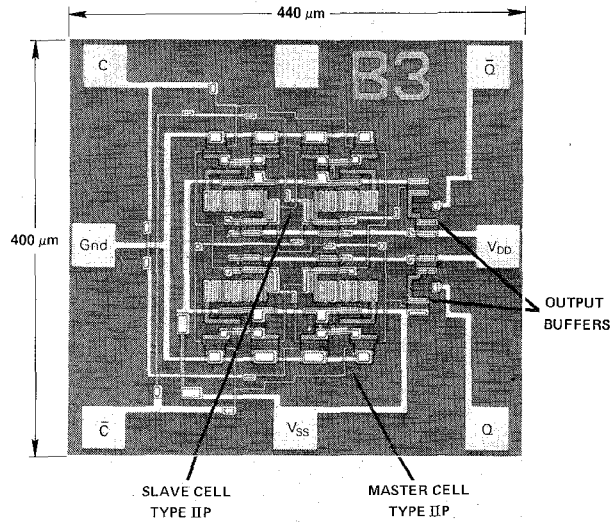

Fig. 6. Master-slave flip-flop frequency divider chip, including two output buffers. Chip size is 400 μm × 440 μm. Characteristic gate width of logic cells is 20 μm.

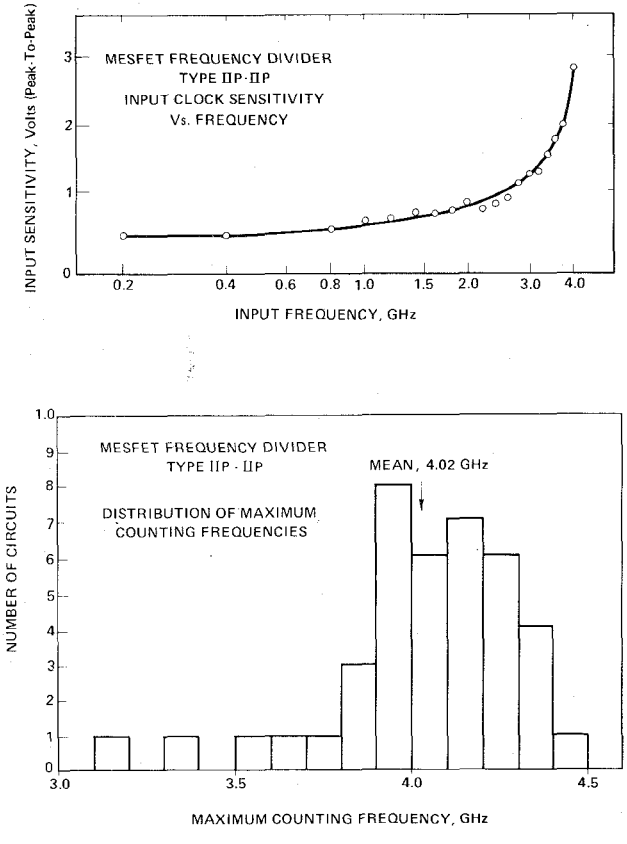

Fig. 7. Response waveforms of master-slave flip-flop binary frequency divider for input frequencies of 5 kHz and 4 GHz.

IIP divider will operate correctly with sinusoidal clock inputs, at fixed dc offset level, from essentially zero frequency to 4 GHz.

Master-slave frequency dividers typically require increased clock amplitude at the higher frequencies. This effect is illustrated in Fig. 8 for the IIP-IIP divider over the input frequency range 200 MHz to 4 GHz. At 200 MHz, 0.6 V, peak-to-peak, is required for correct counting. The drive amplitude requirement increases monotonically to 3 V, peak-to-peak, at 4 GHz, the maximum operating frequency for this particular unit.

The distribution of maximum counting frequencies for all dividers of this particular design on one wafer is shown in Fig. 8(b). The highest speed observation is 4.5 GHz, with a mean maximum counting frequency of 4.0 GHz. This narrow distribution of maximum speeds is made possible by the excel-

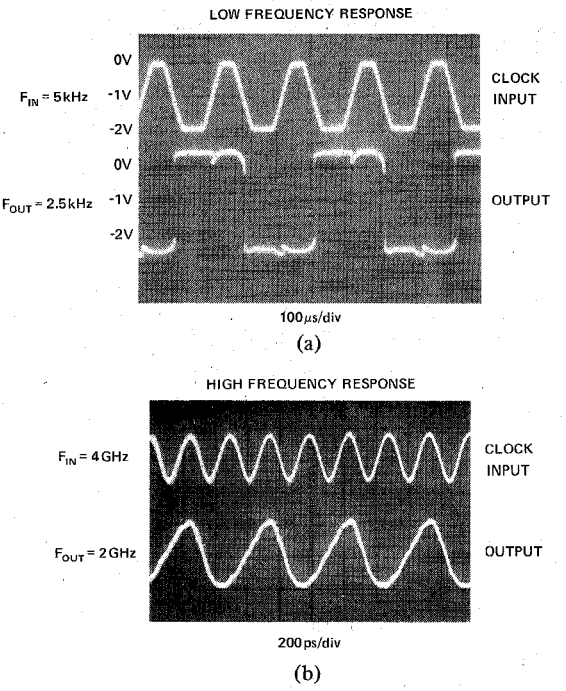

Fig. 8. (a) Input sensitivity of the frequency divider versus frequency. (b) Distribution of maximum counting frequencies for dividers on one wafer.

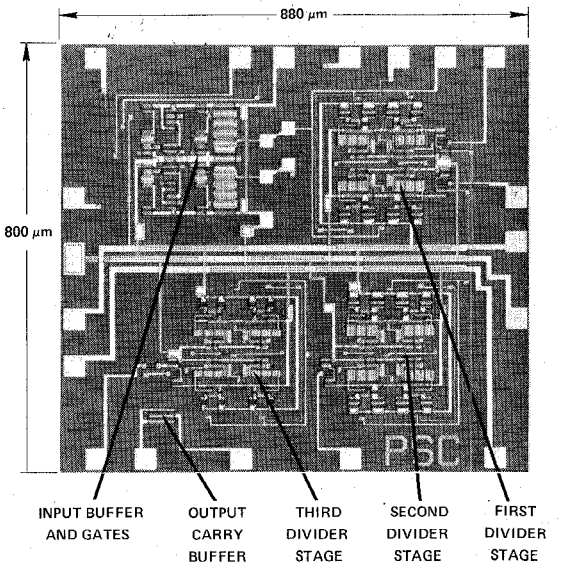

Fig. 9. Counter/timer chip, consisting of input buffer, three binary frequency dividers arranged in a ripple-carry octal divider, and output buffer.

lent uniformity of the selenium-implanted n-layer on this wafer, which resulted in a ±0.5-V worst case variation in V_p. All logic gates on this wafer were at the plateau of maximum speed (unlike the devices shown in Fig. 3), and exhibited only statistical speed variations.

The IIP-IIP divider exhibited a -0.17-percent/C° temperature coefficient, or -340-MHz change in maximum counting frequency for 50°C temperature rise.

V. Medium-Scale Integrated Circuits

Useful application of binary frequency dividers generally requires a combination of several circuits. With the GaAs MESFET technology, where high impedance levels and voltage swings make off-chip connections undesirable, it is particularly important to combine the largest number of circuits possible (consistent with yield and power dissipation limits) on a single chip. Fig. 9 shows a general-purpose divide-by-eight counter

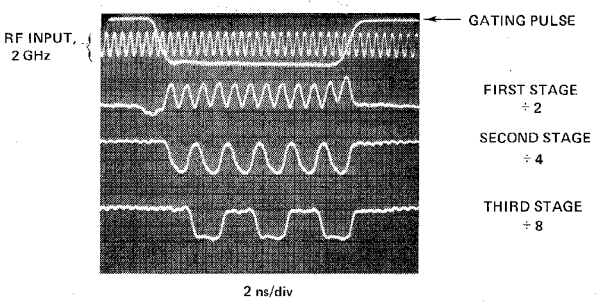

Fig. 10. Waveforms of counter/timer. The gating pulse is 12 ns long, encompassing exactly 24 cycles of the 2-GHz RF input. The prescaler accumulates a count difference of 24 during the gating interval, thereby measuring the pulse duration to an accuracy of ±0.5 ns.

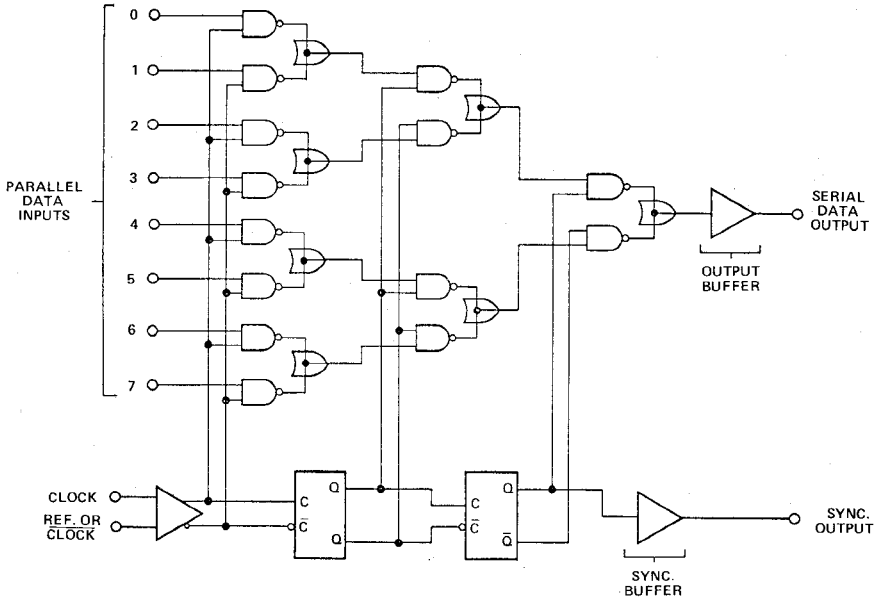

Fig. 11. Logic diagram of an 8-bit multiplexer/data generator.

which consists of three GaAs MESFET binary frequency dividers arranged in a ripple-carry divide-by-eight configuration, a gatable input buffer circuit, and an output buffer for transmitting the divided output signal to lower frequency circuits. Operation of the counter chip is shown in Fig. 10, in which the counter is used to measure the duration of a 12-ns pulse. The pulse, along with a 2-GHz reference frequency, is fed to the input AND gate of the counter chip. The resulting gated burst of RF causes the three stages of the octal divider to respond as shown. The total number of accumulated counts is 24, indicating that the pulse duration is 24 counts × 0.5 ns (period of 2 GHz) = 12 ns. Besides this subnanosecond single-event time-interval measurement, the counter could measure an unknown clock frequency if the gating pulse were of precisely known duration.

Another MSI chip, an 8-bit multiplexer/serial data generator, is shown in the block diagram of Fig. 11. It consists of a divide-by-four counter, a clock input buffer, and an array of seven logic gates arranged in a binary "tree." The three control line pairs derived from the clock buffer and divide-by-four counter progress through eight states as the counter increments. For each of the eight states of these control lines, one "channel" is opened for data to be gated from a particular parallel data input to the serial data output. For instance, if the buffered clock and the "Q" outputs of both flip-flops are all high, then data from parallel input 0 will be allowed to pass through the topmost gates in the first, second, and third ranks to the serial data output. As the divide-by-four counter and buffered clock continue through their eight states (one for each half-cycle of the clock), one parallel data input is selected at a time. The data which are presented in parallel form at the input terminals are thereby converted to a serial bit stream in nonreturn-to-zero (NRZ) form. The data rate of this serial bit stream is twice the clock frequency, since a new bit is presented for each half-cycle of the clock.

Operation of the multiplexer/data generator is illustrated in Fig. 12. Here the serial bit stream "00101011" is generated at data rates of 1, 2, and 3 Gbit/s. The circuit requires an external clock source and an 8-bit parallel data register for inputs. The sampling oscilloscope is triggered by the counter

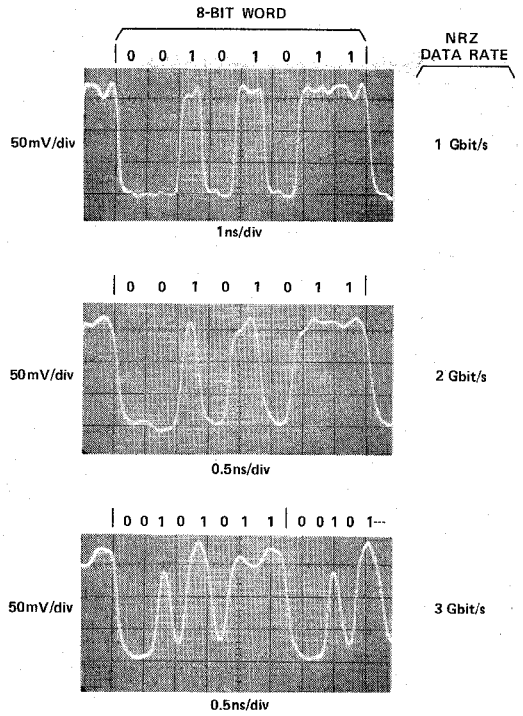

Fig. 12. Multiplexer/data generator operating at nonreturn-to-zero data rates of 1, 2, and 3 Gbit/s.

output, and the serial bit stream appears with a 150-mV amplitude into a 50-Ω load. Certain bit patterns are not correctly generated by the multiplexer. The source of this difficulty is a timing problem which is not completely understood. Nevertheless, the operation, as illustrated in Fig. 12, does show the ability of a MESFET medium-scale IC to perform a useful data-handling function at gigabit rates.

VI. Conclusions

Monolithic GaAs digital IC's with normally-on MESFET's have now reached sufficient maturity that practical and useful electronic functions can be performed. The results presented in this paper show the following features.

1) A practical GaAs IC fabrication technology with two-level metallization enables processing yield of 96 percent per functional logic gate.

2) Satisfactory control of MESFET device parameters can be achieved in the IC fabrication. (For example, the pinchoff voltage can be reproduced from wafer to wafer in the range of $V_p = 2.5\ \text{V} \pm 0.5\ \text{V}$.)

3) NAND/NOR logic gates exhibit 100-ps propagation delay (fan-out = 2) at 40-mW power consumption yielding 4-pJ speed-power product.

4) Frequency dividers with master-slave flip-flops operate at counting rates ranging from dc to 4 GHz.

5) More complex circuits that perform useful logic functions in high-speed measurement or communication systems can be built with reliable and stable operation up to 3-Gbit/s data rate. Examples discussed in this paper were a counter/timer and an 8-bit multiplexer/data generator.

Future developments are aimed toward circuits operating at present speeds but with substantially higher complexity. This objective requires speed-power products below 1 pJ and further improvements in fabrication yield. Smaller circuit size and logic voltage swing, GaAs substrates with higher purity and fewer crystalline defects, and advanced processing techniques such as planar processing, selective implantation, and electron-beam lithography will lead toward this goal. Furthermore, there is a demand for simple circuits with higher speed capability. Significant advancements can also be expected in this area. Computer simulations of improved MESFET logic gates predict 50-ps propagation delay for a fan-out of 2 and a speed-power product of 4 pJ.

This GaAs IC logic family operating at microwave clock frequencies will have a profound effect on the way instruments and systems will be built and will, as well, open the door to completely new applications in the future.

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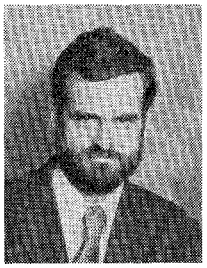

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